



Virtual University

About Us

CS302  
Solved Final Terms Papers

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Year  
2017

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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

In the Name of Allāh, the Most Gracious, the Most Merciful

### Paper Pattern

MCQS 40 each 1 mark  
Short 4 each 2 marks  
Short 4 each 3 marks  
long 4 each 5 marks

Question No : 1 of 52

Marks: 1 (Budgeted Time 1 Min)

Caveman number system is Base \_\_\_\_\_ number system

Answer ( Please select your correct option )

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2

☐

5

☐

correct

10

☐

16

☐

Made by: Waqar Siddhu

Question No : 2 of 52

Marks: 1 (Budgeted Time 1 Min)

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result

Answer ( Please select your correct option )

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1001

☐

0110

☐

correct

1111

☐

1100

☐

Made by: Waqar Siddhu



Question No : 3 of 52

Marks: 1 (Budgeted Time 1 Min)

The Gray code is different from the unsigned binary code because \_\_\_\_\_

Answer ( Please select your correct option )

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☐

Successive values of Gray code differ by only one bit

correct

☐

Gray Code is positional code

☐

Gray Code does not support negative values

☐

Gray Code ranges from "0" to "9"

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Question No : 4 of 52

Marks: 1 (Budgeted Time 1 Min)

"74ALS" stands for \_\_\_\_\_

Answer ( Please select your correct option )

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☐

Advanced Low-frequency Schottky TTL

☐

Advanced Low-dissipation Schottky TTL

☐

Advanced Low-Power Schottky TTL

correct

☐

Advanced Low-propagation Schottky TTL

Made by: Waqar Siddhu

Question No : 5 of 52

Marks: 1 (Budgeted Time 1 Min)

The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

Answer ( Please select your correct option )

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☐

4

☐

8

correct

☐

12

☐

16

Made by: Waqar Siddhu



Question No : 6 of 52

Marks: 1 (Budgeted Time 1 Min)

The cell marked 6 in 4-variable K-Map represent minterm 6 or the maxterm 6 having the following binary value of variables A, B, C and D.

Answer ( Please select your correct option )

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☐ A=1, B=1, C=0, D=0☐ A=0, B=1, C=1, D=0

correct

☐ A=0, B=0, C=1, D=1☐ A=1, B=0, C=0, D=1

Made by: Waqar Siddhu

Question No : 7 of 52

Marks: 1 (Budgeted Time 1 Min)

The PROM consists of a fixed non-programmable \_\_\_\_\_ Gate array configured as a decoder.

Answer ( Please select your correct option )

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☐ AND

correct

☐ OR☐ NOT☐ XOR

Made by: Waqar Siddhu

Question No : 8 of 52

Marks: 1 (Budgeted Time 1 Min)

In a sequential circuit the next state is determined by \_\_\_\_\_ and \_\_\_\_\_

Answer ( Please select your correct option )

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☐ State variable, current state☐ Current state, flip-flop output☐ Current state and external input

correct

☐ Input and clock signal applied

Made by: Waqar Siddhu



Question No : 9 of 52

Marks: 1 (Budgeted Time 1 Min)

In CMOS 5 Volt series, Input voltage for Logic high signal ( $V_{IH}$ ) is in the range of \_\_\_\_\_ volts.

Answer ( Please select your correct option )

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☐ 3.5 to 5

correct

☐ 4.5 to 5

☐ 0 to 5

☐ 0 to 3.5

Made by: Waqar Siddhu

Question No : 10 of 52

Marks: 1 (Budgeted Time 1 Min)

What will be output state when  $J = 1$ ,  $K = 0$  and CLR input is active?

Answer ( Please select your correct option )

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☐  $Q = 1$

correct

☐  $Q = 0$

☐ Retains previous output state

☐ Toggle output

Made by: Waqar Siddhu

Question No : 11 of 52

Marks: 1 (Budgeted Time 1 Min)

A feature that distinguishes JK flip-flop from SR flip-flop is \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Toggle condition

correct

☐ Preset input

☐ Type of clock

☐ Clear input

Made by: Waqar Siddhu

Question No : 12 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following expressions is an example of Commutative Law for Multiplication?

Answer ( Please select your correct option )

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☐  $AB+C = A+BC$ ☐  $A(B+C) = B(A+C)$ ☐  $AB=BA$ ☐  $A+B=B+A$ 

correct

Made by: Waqar Siddhu

Question No : 13 of 52

Marks: 1 (Budgeted Time 1 Min)

The binary values for the standard SOP expression,  $ABCD + \bar{A}BC\bar{D} + \bar{A}\bar{B}CD$  are \_\_\_\_\_

Answer ( Please select your correct option )

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☐  $1110 + 0110 + 0001$ ☐  $1011 + 1111 + 1011$ ☐  $0001 + 1001 + 1110$ ☐  $1010 + 1110 + 0101$ 

correct

Made by: Waqar Siddhu

Question No : 14 of 52

Marks: 1 (Budgeted Time 1 Min)

The design and implementation of synchronous counters start from \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Truth table☐ K-map☐ State table☐ State diagram

correct

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Question No : 15 of 52

Marks: 1 (Budgeted Time 1 Min)

In a state diagram, the transition from a current state to the next state is determined by \_\_\_\_\_ and \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Current state, inputs

correct

☐ Current state, outputs☐ Previous state, inputs☐ Previous state, outputs

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Question No : 16 of 52

Marks: 1 (Budgeted Time 1 Min)

In \_\_\_\_\_, the  $\bar{Q}$  output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

Answer ( Please select your correct option )

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☐ Moore machine☐ Mealy machine☐ Johnson counter

correct

☐ Ring counter

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Question No : 17 of 52

Marks: 1 (Budgeted Time 1 Min)

The sequence of states that are implemented by a n-bit Johnson counter is \_\_\_\_\_

Answer ( Please select your correct option )

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☐  $n+2$  (n plus 2)☐  $2n$  (n multiplied by 2)

correct

☐  $2^n$  (2 raise to power n)☐  $n^2$  (n raise to power 2)

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Question No : 18 of 52

Marks: 1 (Budgeted Time 1 Min)

Flip flops are also called \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Bi-stable dualvibrators

☐ Bi-stable transformer

☐ Bi-stable multivibrators

☐ Bi-stable singlevibrators

correct

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Question No : 19 of 52

Marks: 1 (Budgeted Time 1 Min)

For a gated D-Latch, if  $EN=1$  and  $D=1$  then  $Q(t+1) =$  \_\_\_\_\_

Answer ( Please select your correct option )

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☐ 0

☐ 1

☐  $Q(t)$

☐ Invalid

correct

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Question No : 20 of 52

Marks: 1 (Budgeted Time 1 Min)

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Doesn't have an invalid state

☐ Sets to clear when both  $J = 0$  and  $K = 0$

☐ It does not show transition on change in pulse

☐ It does not accept asynchronous inputs

correct

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Question No : 21 of 52

Marks: 1 (Budgeted Time 1 Min)

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_\_ of the flip-flop.

Answer ( Please select your correct option )

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☐

Set-up time

☐

Pulse Stability time (PST)

☐

Hold time

correct

☐

Pulse Interval time

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Question No : 22 of 52

Marks: 1 (Budgeted Time 1 Min)

The \_\_\_\_\_ input overrides the \_\_\_\_\_ input

Answer ( Please select your correct option )

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☐

Asynchronous, synchronous

correct

☐

Synchronous, asynchronous

☐

Preset input (PRE), clear input (CLR)

☐

Clear input (CLR), preset input (PRE)

Made by: Waqar Siddhu

Question No : 23 of 52

Marks: 1 (Budgeted Time 1 Min)

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

Answer ( Please select your correct option )

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☐

Mod-6, Mod-10

correct

☐

Mod-50, Mod-10

☐

Mod-10, Mod-50

☐

Mod-50, Mod-6

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Question No : 24 of 52

Marks: 1 (Budgeted Time 1 Min)

The hours counter is implemented using \_\_\_\_\_.

Answer ( Please select your correct option )

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☐ Mod-10 and Mod-2 counters

☐ A single decade counter and a flip-flop

correct

☐ Only a single Mod-12 counter is required

☐ Mod-10 and Mod-6 counters

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Question No : 25 of 52

Marks: 1 (Budgeted Time 1 Min)

State Machine is a generic name given to \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Sequential circuits

correct

☐ Combinational circuits

☐ Flip-flops

☐ Counters

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Question No : 26 of 52

Marks: 1 (Budgeted Time 1 Min)

\_\_\_\_\_ is used to simplify the circuit that determines the next state.

Answer ( Please select your correct option )

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☐ State diagram

☐ Next state table

☐ State reduction

☐ State assignment

correct

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Question No : 27 of 52

Marks: 1 (Budgeted Time 1 Min)

The alternate solution for a demultiplexer-register combination circuit is \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Parallel in / Serial out shift register

☐ Serial in / Parallel out shift register

correct

☐ Parallel in / Parallel out shift register

☐ Serial in / Serial Out shift register

Made by: Waqar Siddhu

Question No : 28 of 52

Marks: 1 (Budgeted Time 1 Min)

In the following statement  
Z PIN 20 ISTYPE 'reg invert',  
The keyword "reg invert" indicates \_\_\_\_\_

Answer ( Please select your correct option )

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☐ An inverted register input

☐ An inverted register input at pin 20

☐ Active-high Registered Mode output

☐ Active-low Registered Mode output

correct

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Question No : 29 of 52

Marks: 1 (Budgeted Time 1 Min)

A GAL is essentially a \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Non-reprogrammable PAL

☐ PAL that is programmed only by the manufacturer

☐ Reprogrammable PAL

correct

☐ Reprogrammable PAL

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Question No : 30 of 52

Marks: 1 (Budgeted Time 1 Min)

Which is not characteristic of a shift register?

Answer ( Please select your correct option )

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☐ Serial in/parallel in

correct

☐ Serial in/parallel out

☐ Parallel in/serial out

☐ Parallel in/parallel out

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Question No : 31 of 52

Marks: 1 (Budgeted Time 1 Min)

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

Answer ( Please select your correct option )

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☐ 1100

☐ 0011

☐ 0000

correct

☐ 1111

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Question No : 32 of 52

Marks: 1 (Budgeted Time 1 Min)

A Nibble consists of \_\_\_\_\_ bits

Answer ( Please select your correct option )

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☐ 2

☐ 4

correct

☐ 8

☐ 16

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Question No : 33 of 52

Marks: 1 (Budgeted Time 1 Min)

The address, from which the data is read, is provided by \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Depends on circuitry

☐ None of given options

☐ RAM

☐ Microprocessor

correct

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Question No : 34 of 52

Marks: 1 (Budgeted Time 1 Min)

FIFO is an acronym for \_\_\_\_\_

Answer ( Please select your correct option )

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☐ First In, First Out

correct

☐ Fly in, Fly Out

☐ Fast in, Fast Out

☐ None of given options

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Question No : 35 of 52

Marks: 1 (Budgeted Time 1 Min)

In order to synchronize two devices that consume and produce data at different rates, we can use \_\_\_\_\_

Answer ( Please select your correct option )

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☐ Read Only Memory

☐ First In First Out Memory

correct

☐ Flash Memory

☐ Fast Page Access Mode Memory

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Question No : 36 of 52

Marks: 1 (Budgeted Time 1 Min)

If the FIFO Memory output is already filled with data then \_\_\_\_\_

Answer ( Please select your correct option )

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- ☐ It is locked; no data is allowed to enter
- ☐ It is not locked; the new data overwrites the previous data.
- ☐ Previous data is swapped out of memory and new data enters
- ☐ None of given options

correct

Made by: Waqar Siddhu

Question No : 37 of 52

Marks: 1 (Budgeted Time 1 Min)

The voltage gain of the Inverting Amplifier is given by the relation \_\_\_\_\_

Answer ( Please select your correct option )

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- ☐  $V_{out} / V_{in} = - R_f / R_i$
- ☐  $V_{out} / R_f = - V_{in} / R_i$
- ☐  $R_f / V_{in} = - R_i / V_{out}$
- ☐  $R_f / V_{in} = R_i / V_{out}$

correct

Made by: Waqar Siddhu

Question No : 38 of 52

Marks: 1 (Budgeted Time 1 Min)

The process of converting the analogue signal into a digital representation (code) is known as \_\_\_\_\_

Answer ( Please select your correct option )

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- ☐ Strobing
- ☐ Amplification
- ☐ Quantization
- ☐ Digitization

correct

Made by: Waqar Siddhu



Question No : 39 of 52

Marks: 1 (Budgeted Time 1 Min)

Sampling of an analog signal produces :

Answer ( Please select your correct option )

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☐

A series of impulses those are proportional to the frequency of the signal

☐

A series of impulses those are proportional to the amplitude of the signal

☐

Digital codes that represent the analog signal amplitude

☐

Digital codes that represent the time of each sample

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Question No : 40 of 52

Marks: 1 (Budgeted Time 1 Min)

In a binary-weighted D/A converter, the resistors on the inputs :

Answer ( Please select your correct option )

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☐

Limit the power consumption

☐

Prevent loading on the source

☐

Determine the weights of the digital inputs

☐

Determine the amplitude of the analog signal

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Question No : 41 of 52

Marks: 2 (Budgeted Time 4 Min)

Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations.

Answer ( Please click here to Add Answer )

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Rich text editor toolbar with icons for bold, italic, underline, list, link, unlink, and other formatting options.

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Question No : 42 of 52

Marks: 2 (Budgeted Time 4 Min)

What is meant by state variable?

Answer ( [Please click here to Add Answer](#) )

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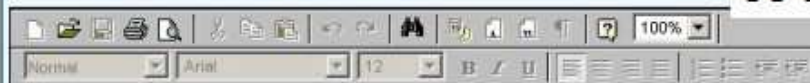
Question No : 43 of 52

Marks: 2 (Budgeted Time 4 Min)

The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. What will be the contents of register after two clock pulses?

Answer ( [Please click here to Add Answer](#) )

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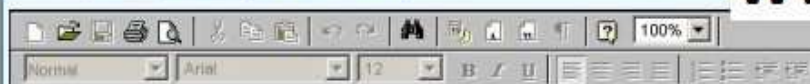
Question No : 44 of 52

Marks: 2 (Budgeted Time 4 Min)

What is the function of row and column decoders?

Answer ( [Please click here to Add Answer](#) )

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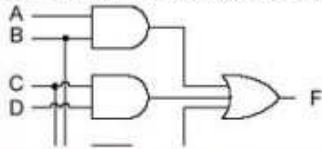
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Question No : 45 of 52

Marks: 3 (Budgeted Time 6 Min)

From the circuit diagram given below derive the output expression.

Answer ( [Please click here to Add Answer](#) )

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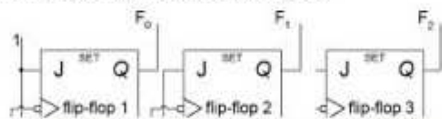


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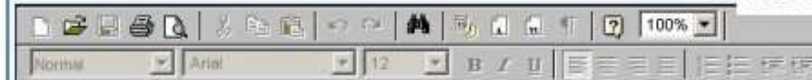
Question No : 46 of 52

Marks: 3 (Budgeted Time 6 Min)

Following is an incomplete circuit of 3-bit Synchronous Down-counter, in which flip-flop 3 is left unconnected. Connect this 3<sup>rd</sup> flip-flop with flip-flop 2 in such a way that functionality of 3-bit Synchronous Down-counter is achieved.

Answer ( [Please click here to Add Answer](#) )

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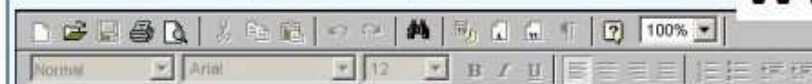
Question No : 47 of 52

Marks: 3 (Budgeted Time 6 Min)

Suppose a 2 bit up-down counter having states "A, B, C, D". The counter counts upward when X=1 and downward when X=0. Write down IF-THEN-ELSE statements to show how present states change to next states and previous states.

Answer ( [Please click here to Add Answer](#) )

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Question No : 48 of 52

Marks: 3 (Budgeted Time 6 Min)

How DRAMs are different from SRAMs? Write three point of differences.

Answer ( [Please click here to Add Answer](#) )

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Question No : 49 of 52

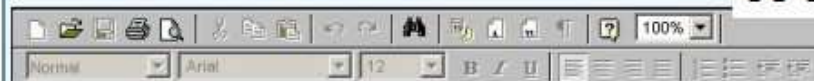
Marks: 5 (Budgeted Time 10 Min)

Using K- map, minimize the following POS expression:

$$(A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + C)$$

Answer ( [Please click here to Add Answer](#) )

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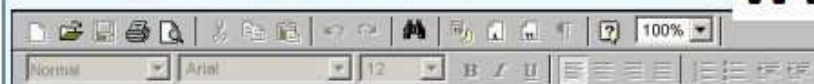
Question No : 50 of 52

Marks: 5 (Budgeted Time 10 Min)

Draw the state diagram of a 3-bit up-down counter. Use an external input X, when X sets to logic 1, the counter counts downward otherwise counts upward.

Answer ( [Please click here to Add Answer](#) )

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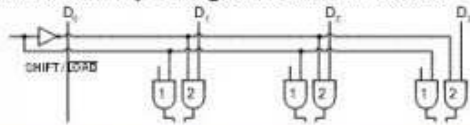
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Question No : 51 of 52

Marks: 5 (Budgeted Time 10 Min)

Given below is an incomplete circuit diagram of parallel in / serial out shift register, in which Q0, Q1, Q2, Q3, and Clock input are disconnected. Connect above mentioned connections in such a way that functionality of the given circuit is not affected.

Answer ( [Please click here to Add Answer](#) )

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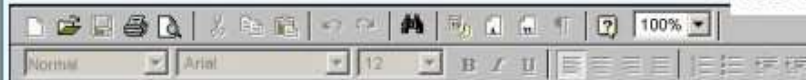
Question No : 52 of 52

Marks: 5 (Budgeted Time 10 Min)

How a registered based LIFO memory is implemented? Draw block diagram of five bytes registered based LIFO memory.

Answer ( [Please click here to Add Answer](#) )

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